

## **CLAIMS**

### **WE CLAIM:**

1. A method for improving high-speed output buffer components comprising the steps of:
  - establishing a cascode transistor module for receiving a substantially differential current signal from a differential pair module and transmitting said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform; and,
  - engineering the resistive loads seen by the output nodes of said differential pair module, based on one or more criteria thereby engineering the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform.
2. The method of claim 1 wherein said cascode transistor module comprises bipolar transistors.
3. The method of claim 1 wherein said cascode transistor module comprises field effect transistors (FETs).
4. The method of claim 1 wherein said differential pair module comprises bipolar transistors.
5. The method of claim 4 wherein said output nodes of said differential pair module comprise the collector nodes of said bipolar transistors and the input nodes of said differential pair module comprise the base nodes of said bipolar transistors.
6. The method of claim 1 wherein said differential pair module comprises field effect transistors (FETs).
7. The method of claim 6 wherein said output nodes of said differential pair module comprise the drain nodes of said field effect transistors (FETs) and the input

nodes of said differential pair module comprise the gate nodes of said field effect transistors.

8. The method of claim 1 wherein the step of engineering the resistive loads comprises the step of inserting a first resistive module between said cascode transistor module and said differential pair module.
9. The method of claim 8 wherein said first resistive module comprises a first resistor and a second resistor in a parallel configuration.
10. The method of claim 9 wherein said first resistor and said second resistor have substantially identical characteristics.
11. The method of claim 1 wherein the step of engineering the resistive loads comprises the step of selecting a cascode bias voltage for said cascode transistor module.
12. The method of claim 11 wherein the step of engineering the resistive loads comprises suppressing the voltages at the outputs of said differential pair module by increasing the maximum range of values for said differential pair module's input voltages and output voltages.
13. The method of claim 11 wherein the step of engineering the resistive loads comprises suppressing the voltages at the outputs of said differential pair module by increasing the degree of non-linearity of the input-output capacitance of the differential pair module transistors as a function of the input-output voltage of said differential pair module transistors.
14. The method of claim 1 further comprising the step of preconditioning the signal input to said differential pair module.
15. The method of claim 14 wherein the step of preconditioning the signal comprises the step of preconditioning the signal input to said differential pair module using one or more stages selected from the list of:
  - an amplifier;
  - a limiting amplifier;
  - a buffer; and

a Cherry-Hooper amplifier.

16. The method of claim 1 further comprising the step of engineering the resistance due to the stage driving the input to said differential pair module.
17. The method of claim 16 wherein the step of engineering the resistance due to the stage driving the input to said differential pair module comprises engineering the symmetry between the rising edge and the falling edge for each of said differential pair module's input voltages supplied to the input nodes of said differential pair module.
18. The method of claim 16 wherein the step of engineering the resistance due to the stage driving the input to said differential pair module comprises one or more steps selected from the list of steps consisting of:
  - coupling a second resistive module to the input node of the first transistor in said differential pair; and,
  - coupling a third resistive module at the input node of the second transistor in said differential pair.
19. The method of claim 18 wherein said second resistive module and said third resistive are substantially identical.
20. The method of claim 18 wherein said second resistive module and said third resistive comprise one or more resistors.
21. The method of claim 1 wherein said pair of external load impedances comprise one or more inductive modules.
22. The method of claim 1 wherein symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform is optimized to achieve a symmetrical output waveform.
23. The method of claim 1 wherein symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform is optimized to achieve an asymmetrical output waveform.
24. An improved high-speed output buffer component comprising:

a cascode transistor module for receiving a substantially differential current signal from a differential pair module and transmitting said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform wherein said cascode transistor module comprises:

a resistive load at the input nodes of said cascode transistor module; and

a cascode bias voltage node for applying a cascode bias voltage wherein the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform may be altered by careful selection of one or more elements selected from the list of:

said resistive load and

said cascode bias voltage.

25. The improved high-speed output buffer component of claim 24 wherein said resistive load at the input nodes of said cascode transistor module are due to the intrinsic properties of the transistor elements.
26. The improved high-speed output buffer component of claim 24 further comprising a first resistive module coupled between said cascode transistor module and said differential pair module for increasing the resistive load at input nodes of said cascode transistor module.
27. The improved high-speed output buffer component of claim 26 wherein said first resistive module comprises a first resistor and a second resistor in a parallel configuration.
28. The improved high-speed output buffer component of claim 27 wherein said first resistor and said second resistor have substantially identical characteristics.
29. The improved high-speed output buffer component of claim 24 wherein said cascode bias voltage is engineered to suppress the voltages at the outputs of said differential pair module.
30. The improved high-speed output buffer component of claim 24 wherein said cascode transistor module comprises bipolar transistors.

31. The improved high-speed output buffer component of claim 24 wherein said cascode transistor module comprises field effect transistors (FETs).
32. The improved high-speed output buffer component of claim 24 wherein said differential pair module comprises bipolar transistors.
33. The improved high-speed output buffer component of claim 32 wherein said output nodes of said differential pair module comprise the collector nodes of said bipolar transistors and the input nodes of said differential pair comprise the base nodes of said bipolar transistors.
34. The improved high-speed output buffer component of claim 24 wherein said differential pair module comprises field effect transistors (FETs).
35. The improved high-speed output buffer component of claim 34 wherein said output nodes of said differential pair module comprise the drain nodes of said field effect transistors (FETs) and said input nodes of said differential pair module comprise the gate nodes of said field effect transistors.
36. The improved high-speed output buffer component of claim 24 further comprising one or more circuit elements selected from the list of:
  - a keep alive transistor and
  - a bleed resistor.
37. The improved high-speed output buffer component of claim 24 wherein:
  - said differential pair module comprises a pair of differential pair module inputs for receiving a differential input signal; and,
  - one or more stages for preconditioning said differential input signal are coupled to said pair of differential pair module inputs.
38. The improved high-speed output buffer component of claim 37 wherein said stages comprise one or more stages selected from the list of:
  - an amplifier;
  - a limiting amplifier;
  - a buffer; and
  - a Cherry-Hooper amplifier.

39. The improved high-speed output buffer component of claim 24 further comprising one or more inductive modules coupled to the outputs of said cascode transistor module.
40. The improved high-speed output buffer component of claim 24 wherein said differential pair module comprises a first transistor with a first input node and a second transistor with a second input node and wherein said improved high-speed output buffer further comprises one or more elements selected from the list consisting of:
- a second resistive module coupled to the input node of said first transistor;
  - and,
  - a third resistive module coupled to the input node of said second transistor;
- thereby engineering the resistance due to the stage driving the input to said differential pair module and thereby engineering the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform.
41. The improved high-speed output buffer component of claim 40 wherein said second resistive module and said third resistive are substantially identical.
42. The improved high-speed output buffer component of claim 40 wherein said second resistive module and said third resistive comprise one or more resistors.
43. A system comprising:
- one or more devices coupled to
  - the improved high-speed output buffer component of claim 24.
44. The system of claim 43 wherein said devices comprise one or more selected from the list of:
- broad-band amplifiers;
  - high-speed logic gates;
  - narrow-band amplifiers;
  - amplifiers;

logic gates;  
mixers; and  
oscillators.

45. The system of claim 43 wherein said system comprises one or more selected from the list of :

wireless local area networks;  
networks;  
satellite communications devices;  
communications systems;  
global positioning systems; and  
high-speed communication systems.